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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,291	07/23/2003	Richard W. Adkisson	200300032-2	7891
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HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400				
			EXAMINER	
			C'HAN, SAI MING	
			ART UNIT	PAPER NUMBER
			2616	
			NOTIFICATION DATE	DELIVERY MODE
			08/20/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/625,291	Applicant(s) ADKISSON ET AL.
	Examiner Sai-Ming Chan	Art Unit 2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 5/6/2008.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-16 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____
- 5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating

obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3-7, 10 & 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Shin et al. (U.S. Patent Publication # 20040004975)**, in view of **Jones et al. (U.S. Patent Publication # 20030204555)**, and in view of **Arimilli et al. (U.S. Patent # 6874063)**.

Consider **claim 1**, Shin et al. clearly disclose and show a system for effectuating the transfer of data blocks including a header block (fig. 4 (410), fig. 5 (500 header); paragraph 9 (header)) across a clock boundary (paragraph 0009 (transmitter's and receiver's clock domains)) between a first clock domain (paragraph 9 (transmitter's clock domain)) and a second clock domain (paragraph 9 (receiving device's local clock frequency)), wherein said first clock domain is operable with a first clock signal (paragraph 9 (transmitter's clock domain)) and said second clock domain is operable with a second clock signal (paragraph 9 (receiving device's local clock frequency)), said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein $N/M>1$ (paragraph 73 (transmitter's frequency is faster than the receiver's (an overrun condition))), comprising:

a first circuit portion (fig. 2 (201 transmitter; fig. 3)) for providing said data blocks including said header block to a second circuit portion (fig. 2 (202 receiver; fig. 3)); control logic associated with said second circuit portion for processing said header block (fig.3; paragraphs 3 and 83 (control the transmission and reception of the symbols)), and a synchronizer (paragraph 0009 (send signal so that receiver can synchronize with the transmitter)).

However, Shin et al. do not specifically disclose the sending of hint signal across clock boundary.

In the same field of endeavor, Jones et al. clearly shows the sending of hint signal that gives advance notification of a possible data transfer operation (fig. 10 (724), paragraph 0129 (hints for transfer)), wherein the first circuit portion and second circuit portion and said control logic (fig. 7, paragraph 0122) are disposed in said first clock domain (fig. 10 (724)) and said third circuit portion and said control block are disposed in said second clock domain (fig. 10 (726 (send hints to another digital processing system)), paragraph 0135).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to demonstrate a system for data transfer, as taught by Shin et al., and incorporate the hint signal, as taught by Jones et al., so that appropriate element would be selected.

However, Shin et al., as modified by Jones, do not specifically disclose the ordering of data transfer.

In the same field of endeavor, Arimilli et al. clearly shows the ordering of data transfer (abstract (order bit for transmitting data in that order)).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to demonstrate a system for data transfer, as taught by Shin et al., and incorporate hint signal, as taught by Jones et al., and ordering of data transfer, as taught by Arimilli, so that data transfer between two clock domains is done efficiently.

Consider **claims 10 and 13**, Shin et al. clearly disclose and show a method for effectuating the transfer of data blocks including a header block (fig. 4 (410), fig. 5 (500 header); paragraph 9 (header)) across a clock boundary between a first clock domain (paragraph 9 (transmitter's clock domain)) and a second clock domain (paragraph 9 (receiving device's local clock frequency)), wherein said first clock domain is operable with a first clock signal (CLK1) and said second clock domain is operable with a second Clock signal (CLK2), comprising:

processing a header block associated with data blocks (fig. 4 (410), fig. 5 (500 header); paragraph 9 (header)) that are to be sent from said first clock domain (paragraph 9 (transmitter's clock domain)) to said second clock domain (paragraph 9 (receiving device's local clock frequency)) via a synchronizer (paragraph 0009 (send signal so that receiver can synchronize with the transmitter));

However, Shin et al. do not specifically disclose the sending of hint signal across clock boundary.

generating a hint signal (fig. 10 (724), paragraph 0129 (hints for transfer)) responsive to said header block (paragraph 0011 (header)) and positioning said hint signal at least one cycle prior to the location of said data blocks (fig. 3 (307 (media files following hints)), paragraph 0129 (hints for transfer));

transmitting said hint signal to a control block (fig. 10 (726 (send hints to another digital processing system))) in said second clock domain (fig. 10 (726 (send hints to another digital processing system))), thereby indicating that said data blocks may be sent to receive circuitry in said second clock domain (fig. 10 (726 (send hints to another digital processing system)), paragraph 0135);

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to demonstrate a system for data transfer, as taught by Shin et al., and incorporate the hint signal, as taught by Jones et al., so that appropriate element would be selected.

However, Shin et al., as modified by Jones, do not specifically disclose generating appropriate control signals based on said hint signal for controlling output of said data blocks in a particular ordered grouping.

In the same field of endeavor, Arimilli et al. clearly shows generating appropriate control signals based on said hint signal for controlling output of said data blocks in a particular ordered grouping (abstract (order bit for transmitting data in that order)).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to demonstrate a system for data transfer, as taught by Shin et al., and incorporate hint signal, as taught by Jones et al., and ordering of data

transfer, as taught by Arimilli, so that data transfer between two clock domains is done efficiently.

Consider **claim 3**, and **as applied to claim 1 above**, Shin et al., as modified by Jones and Arimilli, clearly disclose and show a system for effectuating the transfer of data blocks including a header block, wherein said first circuit portion comprises a packet interface (fig. 7, paragraph 94 (segmentation of data packet)).

Consider **claims 4**, and **as applied to claim 1 above**, and
claim 14, and **as applied to claim 13 above**,

Shin et al., as modified by Jones and Arimilli, clearly disclose and show a system for effectuating the transfer of data blocks including a header block, wherein said second circuit portion comprises: at least one queue (fig.10 (control (1010) and data (1020) queues; paragraph 109)) operably coupled to said first circuit portion for temporarily storing said data blocks; and a multiplexer (MUX) block (fig. 41(4102), paragraph 173) operably coupled to said first circuit portion and said at least one queue, said MUX block operating under a MUX selection control signal (fig. 41(4102), paragraph 175 (receive uHF and uPTR signals from Pointer Tracker)) generated by said control logic for selecting between data blocks stored in said at least one queue and data blocks provided by said first circuit portion without queuing, whereby said data blocks are transmitted as an output of said MUX block to said synchronizer (fig. 3 (305

frame aligner), fig. 41 (4100 frame aligner), paragraph 173 (4103 sync and null detector)).

Consider **claim 5**, and as applied to claim 1 above, Shin et al., as modified by Jones and Arimilli, clearly disclose and show a system for effectuating the transfer of data blocks including a header block, wherein said third circuit portion comprises means for selecting (fig 13 (1302, 1303), paragraph 113(packet preemption))) between data blocks directly transmitted by said synchronizer (paragraph 174 (symbol pointer tracker)) and data blocks buffered in said second clock domain (fig. 13 (1301, 1305)), said means operating responsive to at least a portion of said data transfer control signals(preempt primitive).

Consider **claim 6**, and as applied to claim 1 above, Shin et al., as modified by Jones and Arimilli, clearly disclose and show a system for effectuating the transfer of data blocks including a header block, wherein said header block provides protocol control information (fig.4 (416 & 417), paragraph 85, lines 13-16) relative to said data blocks.

Consider **claim 7**, and as applied to claim 1 above, Shin et al., as modified by Jones and Arimilli, clearly disclose and show a system for effectuating the transfer of

data blocks including a header block, wherein each of said data blocks comprises multiple bits(paragraph 9 (short block (32 bytes))).

Claims 2, 8, 9, 11-12 & 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Shin et al. (U.S. Patent Publication # 20040004975)**, in view of **Jones et al. (U.S. Patent Publication # 20010040908)**, and in view of **Arimilli et al. (U.S. Patent # 6874063)**, and further in view of **Naumann et al. (U.S. Patent Publication # 20040024946)**.

Consider **claims 2, and as applied to claim 1 above,**
claim 11, and as applied to claim 10 above,
claim 12, and as applied to claim 11 above,
claim 15, and as applied to claim 13 above, and
claim 16, and as applied to claim 15 above

Shin et al., as modified by Jones and Arimilli, clearly disclose and show a system for effectuating the transfer of data blocks including a header block, further comprising a synchronizer controller (fig. 39b, paragraph 171 (CDR - clock and data recover)) disposed between said first and second clock domains for providing at least one dead cycle control signal (paragraph 171(1-bit control signal for inserting null symbol in RX-DA), paragraph 172) to said second circuit portion.

However, Shin et al., as modified by Jones et al., do not specifically disclose the location of the dead cycle in the data flow. In addition, Naumann et al. clearly disclose the location of at least one dead cycle (fig. 20, destination 2, FD2_DATA (A0A1A2A3A4(3 dead cycles)B0B1B2B3B4C0C1C2C3); paragraph 107(3 dead cycles between data flow)).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to demonstrate a system for data transfer, as taught by Shin et al., and incorporate the dead cycles, as taught by Naumann et al., so that data transfer between two clock domains is done efficiently.

Consider **claims 8 & 9, and as applied to claim 1 above**, Shin et al., as modified by Jones and Arimilli, clearly disclose and show a system for effectuating the transfer of data blocks including a header block as described. However, Shin et al., as modified by Jones et al., do not specifically disclose interleaved data block. Furthermore, Naumann et al. clearly disclose data block are interleaved (fig. 20, destination 2, FD2_DATA (A0A1A2A3A4(3 dead cycles)B0B1B2B3B4C0C1C2C3), data flow can be interleaved).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to demonstrate a system for data transfer, as taught by Shin et al., and incorporate interleaved data block, as taught by Naumann et al., so that data transfer between two clock domains is done efficiently.

Response to Amendment

Applicant's arguments filed on 5/6/2008, with respect to claims 1, 10 and 13, on pages 12-21 of the remarks, have been carefully considered.

In the present application, Applicants basically argue, that Shin et al. do not teach or suggest "sending of hint signal across clock boundary". The Examiner has modified the response with a new reference which combines with Shin to provide "sending of hint signal across clock boundary". See the above rejections of claims 1, 10 and 13, for the relevant interpretation and citations found in Jones et al., disclosing the limitations.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any response to this Office Action should be **faxed to (571) 273-8300 or mailed to:**

Commissioner for Patents
P.O. Box 1450
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Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Sai-Ming Chan whose telephone number is (571) 270-1769. The Examiner can normally be reached on Monday-Thursday from 6:30am to 5:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 571-272-4100.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

/Sai-Ming Chan/

Examiner, Art Unit 2616

August 13, 2008

/Kevin C. Harper/

Primary Examiner, Art Unit 2616